

- Advanced Process Technology
- Surface Mount
- Optimized for 4.5V-7.0V Gate Drive
- Ideal for CPU Core DC-DC Converters
- Fast Switching
- Lead-Free

Description

These HEXFET Power MOSFETs were designed specifically to meet the demands of CPU core DC-DC converters. Advanced processing techniques combined with an optimized gate oxide design results in a die sized specifically to offer maximum efficiency at minimum cost.

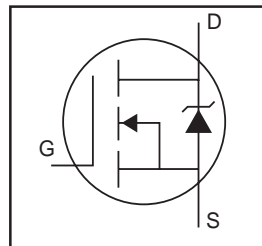
The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

Absolute Maximum Ratings

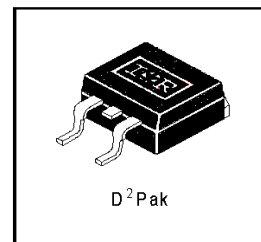
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}^{\text{⑤}}$	61	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}^{\text{⑤}}$	39	
I_{DM}	Pulsed Drain Current ①⑤	240	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	89	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy②⑤	220	mJ
I_{AR}	Avalanche Current①	35	A
E_{AR}	Repetitive Avalanche Energy①	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

Thermal Resistance

	Parameter	Typ.	Max.	Units
R_{qJC}	Junction-to-Case	---	1.4	°C/W
R_{qJA}	Junction-to-Ambient (PCB Mounted, steady-state)**	---	40	



$V_{DSS} = 20\text{V}$
$R_{DS(on)} = 0.013\Omega$
$I_D = 61\text{A}$



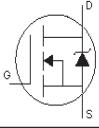
IRL3102SPbF

International
IR Rectifier

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$DV_{(BR)DSS}/DT_J$	Breakdown Voltage Temp. Coefficient	—	0.016	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1mA$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.015	Ω	$V_{GS} = 4.5V, I_D = 37A$ ④
		—	—	0.013		$V_{GS} = 7.0V, I_D = 37A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	0.70	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	36	—	—	S	$V_{DS} = 16V, I_D = 35A$ ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 20V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 10V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 10V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -10V$
Q_g	Total Gate Charge	—	—	58	nC	$I_D = 35A$
Q_{gs}	Gate-to-Source Charge	—	—	14		$V_{DS} = 16V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	21		$V_{GS} = 4.5V$, See Fig. 6 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 10V$
t_r	Rise Time	—	130	—		$I_D = 35A$
$t_{d(off)}$	Turn-Off Delay Time	—	80	—		$R_G = 9.0\Omega, V_{GS} = 4.5V$
t_f	Fall Time	—	110	—		$R_D = 0.28\Omega$ ④⑤
L_S	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C_{iss}	Input Capacitance	—	2500	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	1000	—		$V_{DS} = 15V$
C_{rss}	Reverse Transfer Capacitance	—	360	—		$f = 1.0\text{MHz}$, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	61	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	240		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 37A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	59	88	ns	$T_J = 25^\circ\text{C}, I_F = 35A$
Q_{rr}	Reverse Recovery Charge	—	110	160	nC	$di/dt = 100A/\mu s$ ④⑤
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.36\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 35A$.
- ③ $I_{SD} \leq 35A$, $di/dt \leq 100A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRL3102 data and test conditions

** When mounted on FR-4 board using minimum recommended footprint.
For recommended footprint and soldering techniques refer to application note #AN-994.

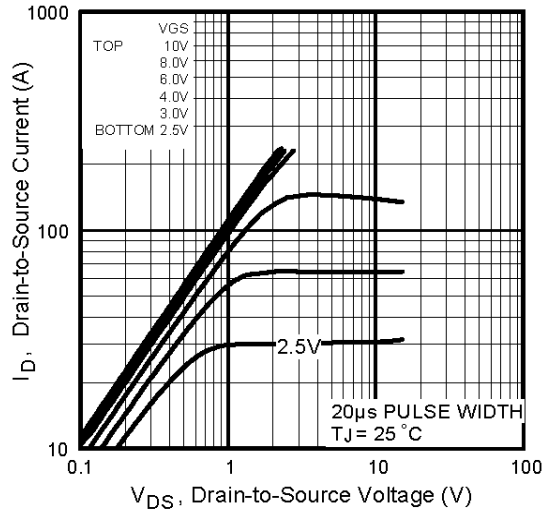


Fig 1. Typical Output Characteristics

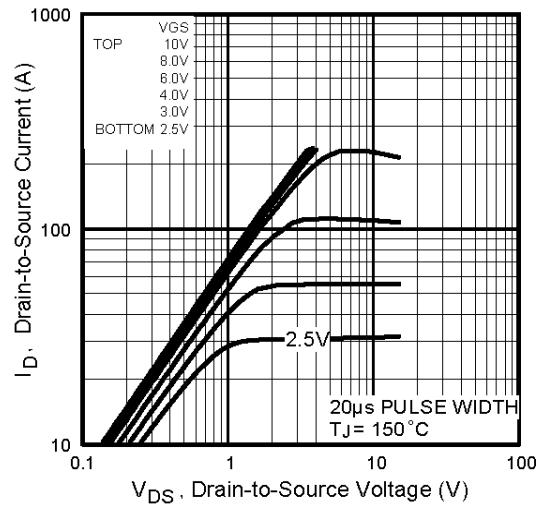


Fig 2. Typical Output Characteristics

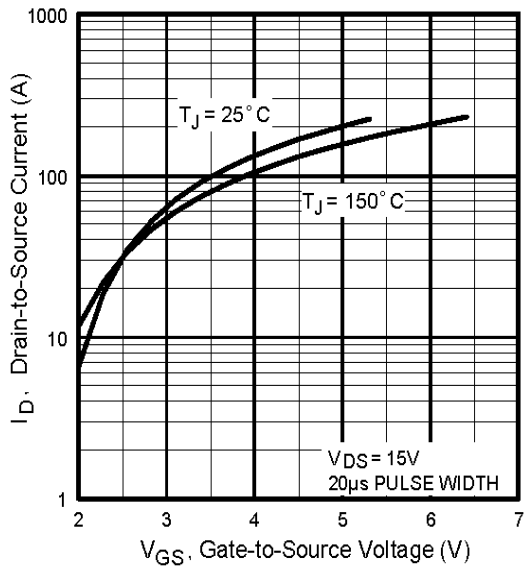


Fig 3. Typical Transfer Characteristics

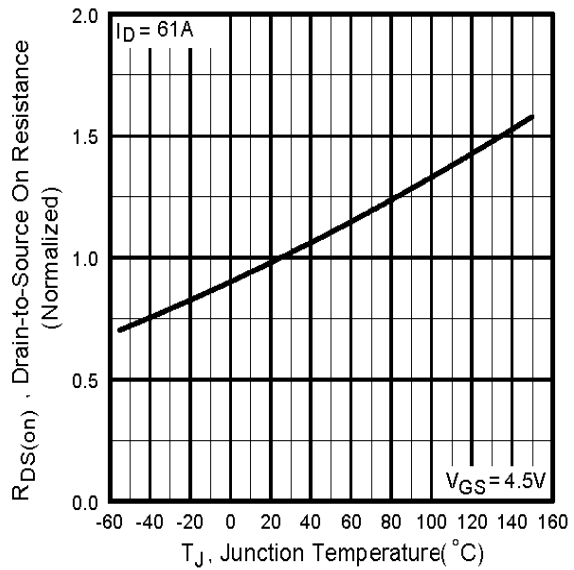


Fig 4. Normalized On-Resistance Vs. Temperature

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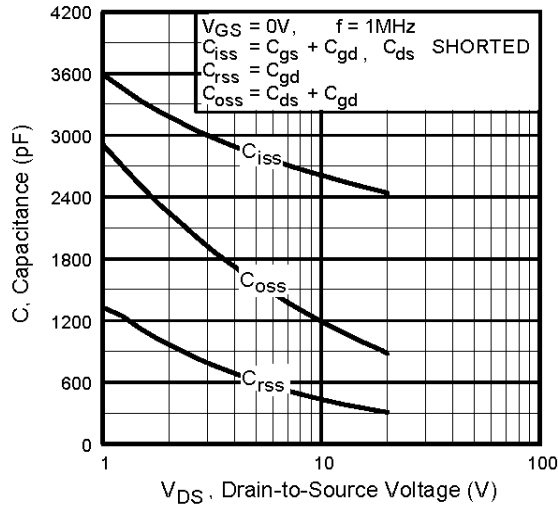


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

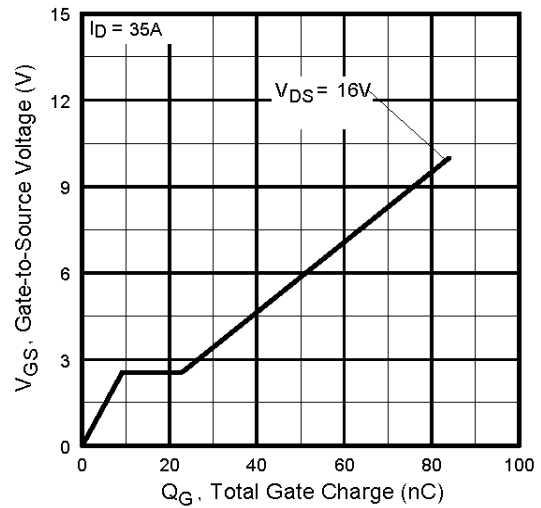


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

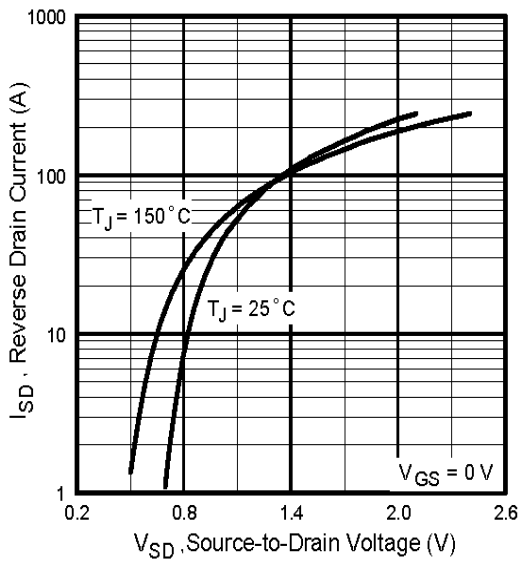


Fig 7. Typical Source-Drain Diode Forward Voltage

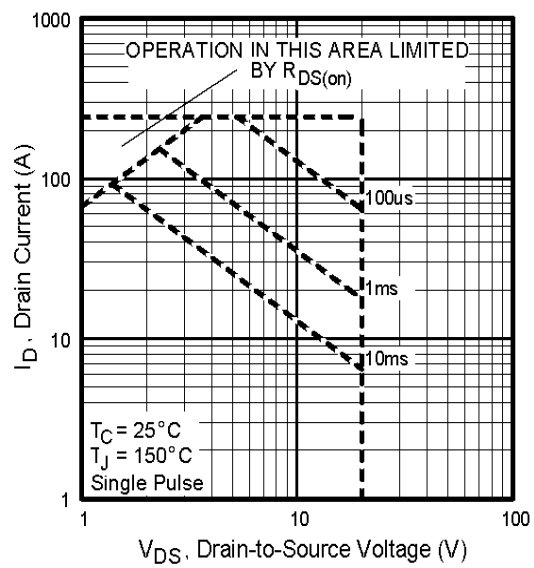


Fig 8. Maximum Safe Operating Area

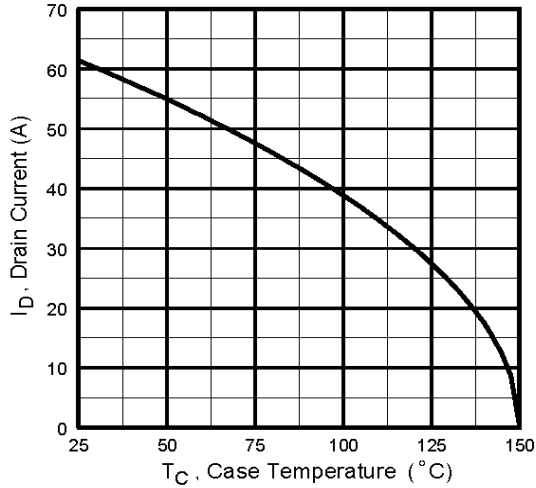


Fig 9. Maximum Drain Current Vs. Case Temperature

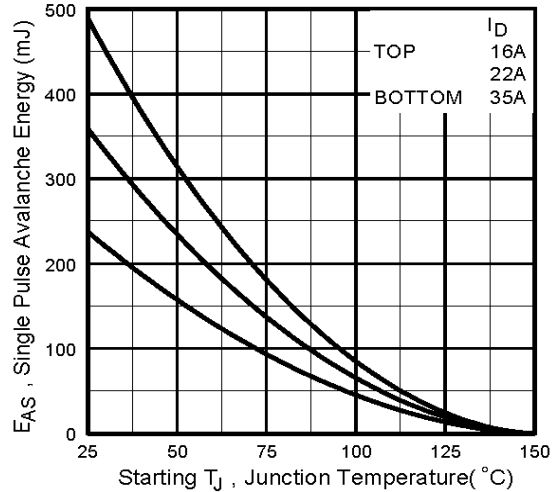


Fig 10. Maximum Avalanche Energy Vs. Drain Current

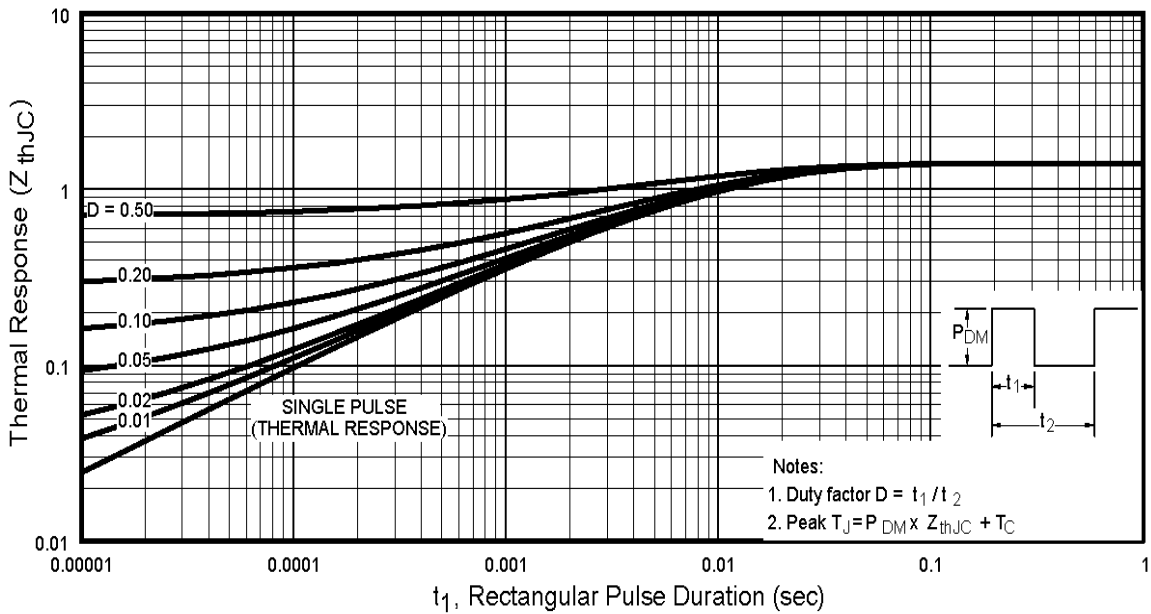


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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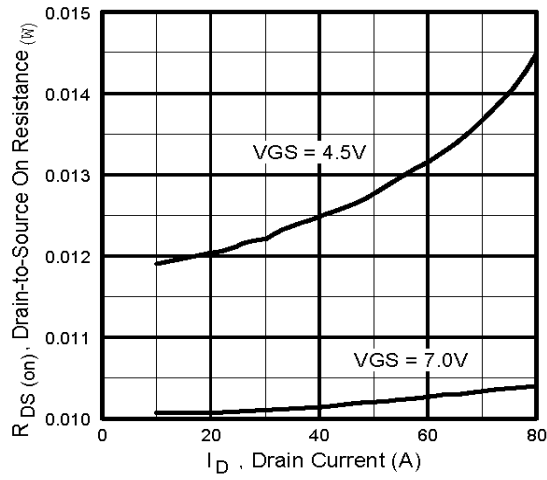


Fig 12. On-Resistance Vs. Drain Current

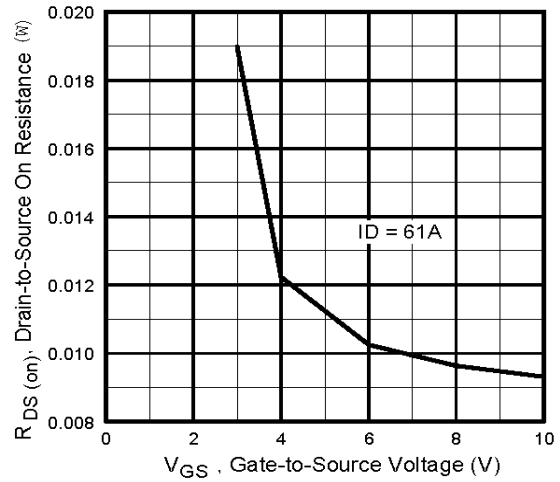
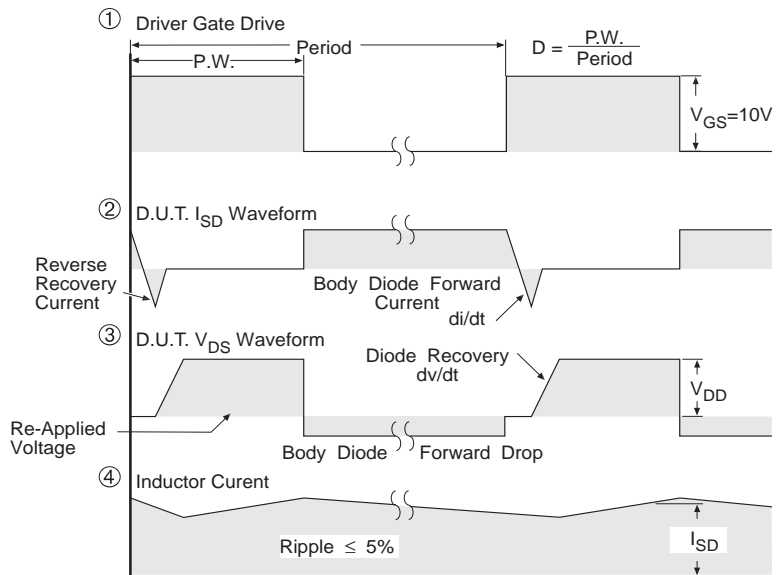


Fig 13. On-Resistance Vs. Gate Voltage

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel
** Use P-Channel Driver for P-Channel Measurements



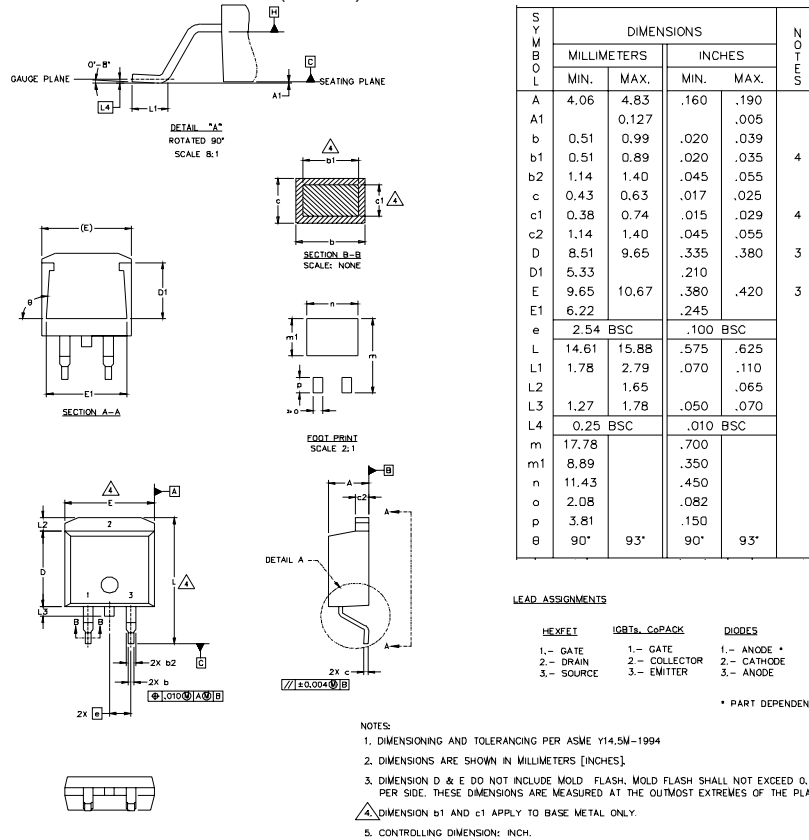
*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14 For N Channel HEXFETS

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D²Pak Package Outline

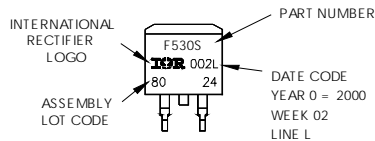
Dimensions are shown in millimeters (inches)



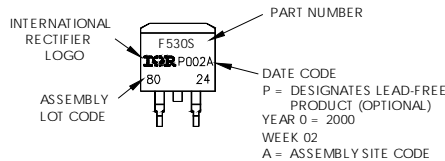
D²Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
position indicates "Lead-Free"

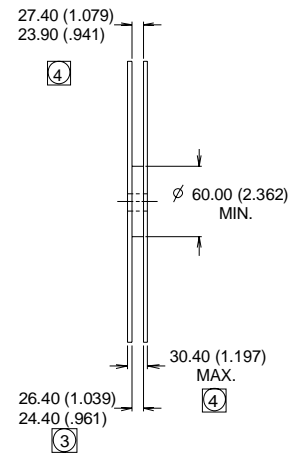
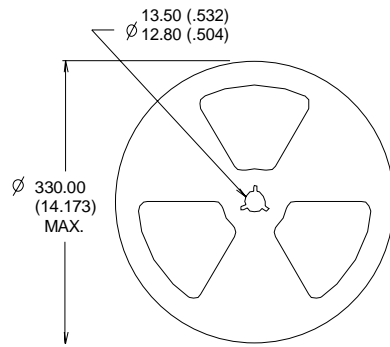
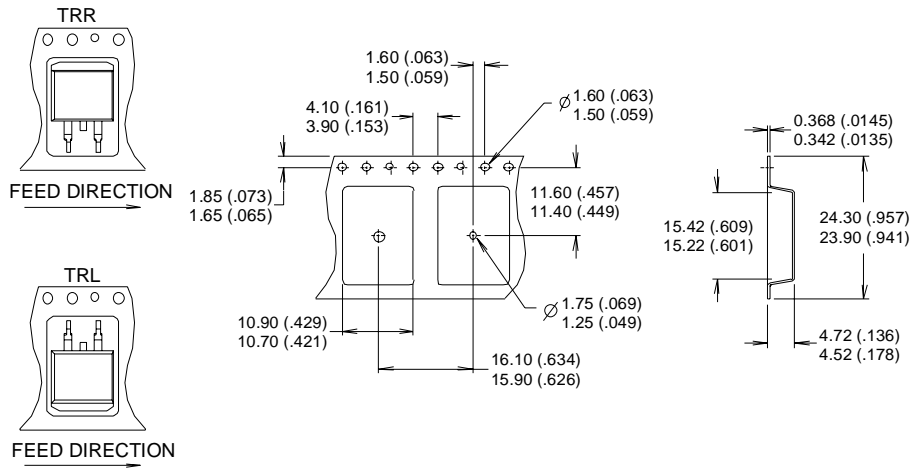


OR



D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONFORMS TO EIA-418.
 2. CONTROLLING DIMENSION: MILLIMETER.
 - ③ DIMENSION MEASURED @ HUB.
 - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>